REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 2 and 3 are now in the application. Claim 1 has been canceled. Claims 2 and 3 have been added.

Claim 2 is supported in the original claim 1 and in the written specification. Specific reference is had to the description of the inventive process from page 7, line 23, to page 9, line 9. As explained there, the memory address test according to the invention is carried out in a two cycle process in parallel with the memory cell access. In a first cycle that corresponds to a row activation, the row address and the bank address are analyzed and an activation pulse is obtained. In the second cycle that corresponds to a column access, the column address is analyzed and a hit signal is output if a faulty memory cell address is detected.

Claim 3 is supported in the specification as well. The device claim is substantially a "picture claim" describing the figure of the drawing. Reference is also had to the description of page 5, line 19, to page 7, line 21.

We now turn to the art rejection, in which claim 1 has been rejected as being anticipated by Deas (US 6,041,422) under 35 U.S.C. § 102. We respectfully traverse on the basis of the amended claims.

Deas discloses a method for the address detection and a corresponding circuit. The

address test operation is carried out as a multi-stage process in which the known defect addresses are latched from an EEPROM into an associated store. In a first state and in a second state the defect addresses are compared with the applied address to detect an address match.

The prior art reference does not teach carrying out the test operation in parallel to the memory cell access in a two cycle process, wherein the row address and the bank address are tested and an activation signal is generated during the first cycle, and wherein the column address is tested and the hit signal is outputted in the second circle.

The prior art reference also does not disclose a circuit structure as it is recited in claim 3. Specifically, Deas does not show or suggest a "third logic stage" with three inputs (an input from the RA:RA_fail comparator, an input from the BA:BA_fail comparator, and an input from the latch whose output signal is subject to two upstream logic stages).

Deas does not anticipate the invention defined in claims 2 and 3. Neither Deas nor any other reference of record, whether taken alone or in any combination, either shows or suggests the features of claims 2 and/or 3.

In view of the foregoing, reconsideration and allowance of claims 2 and 3 are solicited.

No monies are believed to be due with this amendment. Should any amount be due, counsel authorizes the Office to charge such amount to the deposit account No. 12-1099 of Lerner Greenberg Stemer LLP. If an extension of time is required, petition for extension is herewith made.

Respectfully submitted,

For Applicant(s)

WHS:bb

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